

## **FEATURES**

- **Single Power Supply Operation**
  - Low voltage range: 2.7 V - 3.6 V
- **Memory Organization**
  - Pm25LV512A: 64K x 8 (512 Kbit)
  - Pm25LV010A: 128K x 8 (1 Mbit)
  - Pm25LV020: 256K x 8 (2 Mbit)
  - Pm25LV040: 512K x 8 (4 Mbit)
- **Cost Effective Sector/Block Architecture**
  - 512Kb : Uniform 4Kbyte sectors / Two uniform 32Kbyte blocks
  - 1Mb : Uniform 4Kbyte sectors / Four uniform 32Kbyte blocks
  - 2Mb : Uniform 4Kbyte sectors / Four uniform 64Kbyte blocks
  - 4Mb : Uniform 4Kbyte sectors / Eight uniform 64Kbyte blocks
  - Bottom sector is configurable as one 4Kbyte sector or four 1Kbyte sectors (except Pm25LV512A)
- **Serial Peripheral Interface (SPI) Compatible**
  - Supports SPI Modes 0 (0,0) and 3 (1,1)
  - Maximum 33 MHz clock rate for normal read
  - Maximum 100 MHz clock rate for fast read
- **Page Program (up to 256 Bytes) Operation**
  - Typical 2 ms per page program
- **Sector, Block or Chip Erase Operation**
  - Typical 40 ms sector, block or chip erase
- **Software Write Protection**
  - The Block Protect (BP2, BP1, BP0) bits allow partial or entire memory to be configured as read-only
- **Hardware Write Protection**
  - Protect and unprotect the device from write operation by Write Protect (WP#) Pin
- **Low Power Consumption**
  - Typical 10 mA active read current
  - Typical 15 mA program/erase current
- **High Product Endurance**
  - Guarantee 200,000 program/erase cycles per single sector
  - Minimum 20 years data retention
- **Industrial Standard Pin-out and Package**
  - 8-pin 150mil SOIC
  - 8-pin 208mil SOIC for Pm25LV040
  - 8-contact WSON

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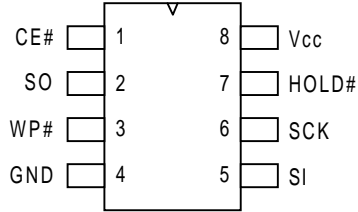
## **GENERAL DESCRIPTION**

The Pm25LV512A/010A/020/040 are 512Kbit/1 Mbit/2 Mbit/4 Mbit 3.0 Volt-only Serial Peripheral Interface (SPI) Flash memories. The devices are designed to support 33 MHz fastest clock rate in the industry in normal read mode, 100 MHz in fast read mode and the bottom 4 Kbyte sector into four smaller 1 Kbyte sectors features(except Pm25LV512A). The devices use a single low voltage, ranging from 2.7 Volt to 3.6 Volt, power supply to perform read, erase and program operations. The devices can be programmed in standard EPROM programmers as well. The Pm25LV512A/010A is backward compatible to their predecessors Pm25LV512/010.

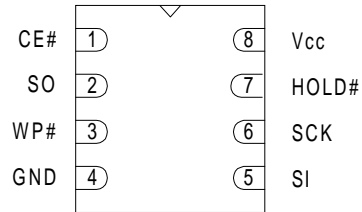
The Pm25LV512A/010A/020/040 are accessed through a 4-wire SPI Interface consists of Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. The devices support page program mode, 1 to 256 bytes data can be programmed into the memory in one program operation. The memory of Pm25LV512A/010A is divided into uniform 4 Kbyte sectors or uniform 32 Kbyte blocks (sector group - consists of eight adjacent sectors) for data or code storage. The memory of Pm25LV020/040 are divided into uniform 4 Kbyte sectors or uniform 64 Kbyte blocks (sector group - consists of sixteen adjacent sectors). The devices have an innovative feature to configure the bottom 4 Kbyte sector into four smaller 1 Kbyte sectors for eliminating additional serial EEPROM needed for storing data. This is a further cost reduction for overall system.

The Pm25LV512A/010A/020/040 are manufactured on pFLASH™'s advanced nonvolatile technology. The devices are offered in 8-pin SOIC and 8-contact WSON packages with operation frequency up to 100 MHz in fast read and 33 MHz in normal read mode.

**CONNECTION DIAGRAMS**



**8-Pin SOIC**

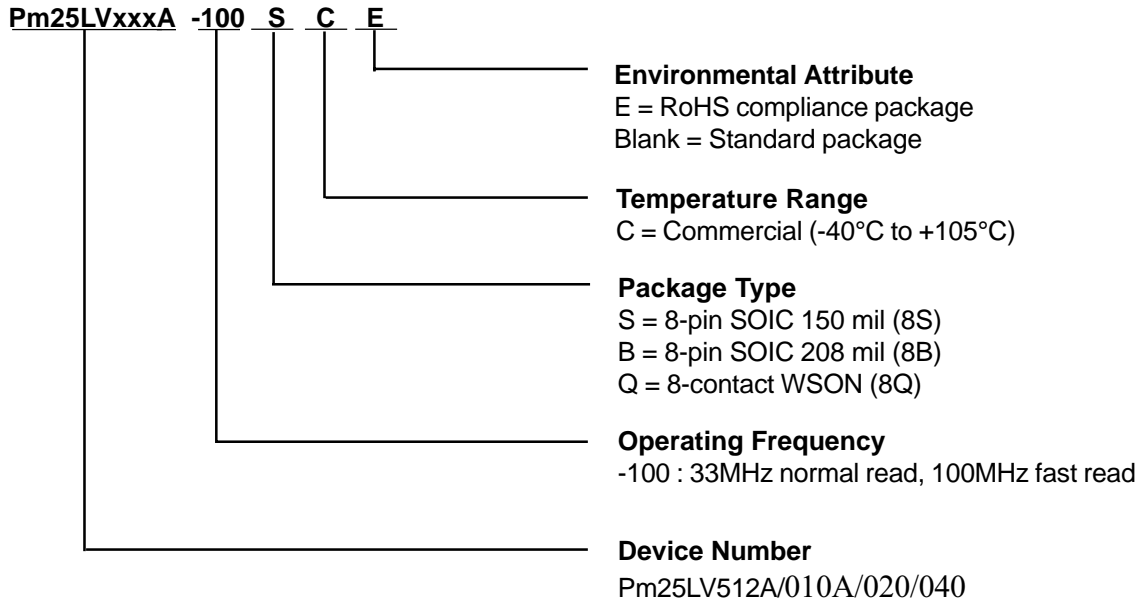


**8-Contact WSON**

**PIN DESCRIPTIONS**

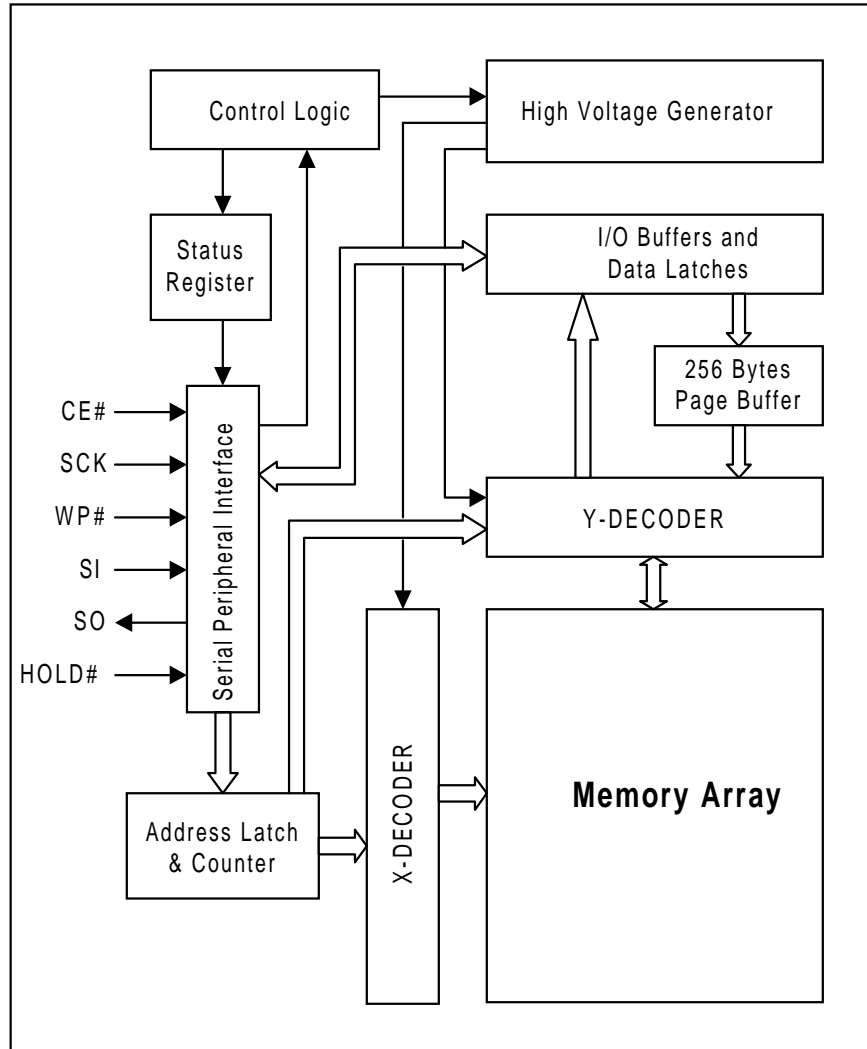
SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Chip Enable: CE# goes low activates the devices internal circuitries for device operation. CE# goes high deselects the devices and switches into standby mode to reduce the power consumption. When the devices are not selected, data will not be accepted via the serial input pin (SI), and the serial output pin (SO) will remain in a high impedance state.
SCK	INPUT	Serial Data Clock
SI	INPUT	Serial Data Input
SO	OUTPUT	Serial Data Output
GND		Ground
Vcc		Device Power Supply
WP#	INPUT	Write Protect: A hardware program/erase protection for all or partial of memory array. When the WP# pin is pulled to low, whole or partial of memory array is write protected depends on the setting of BP2, BP1 and BP0 bits in the Status Register. When the WP# is pulled high, the devices are not write protected.
HOLD#	INPUT	Hold: Pause serial communication with the master device without resetting the serial sequence.

**PRODUCT ORDERING INFORMATION**



Part Number	Operating Frequency (MHz)	Package	Temperature Range
Pm25LV512A-100SCE	100	8S 150mil SOIC	Commercial (-40°C to +105°C)
Pm25LV010A-100SCE			
Pm25LV020-100SCE			
Pm25LV040-100SCE			
Pm25LV512A-100QCE	100	8Q WSON	
Pm25LV010A-100QCE			
Pm25LV020-100QCE			
Pm25LV040-100QCE			
Pm25LV040-100BCE	100	8B 208mil SOIC	

**BLOCK DIAGRAM**



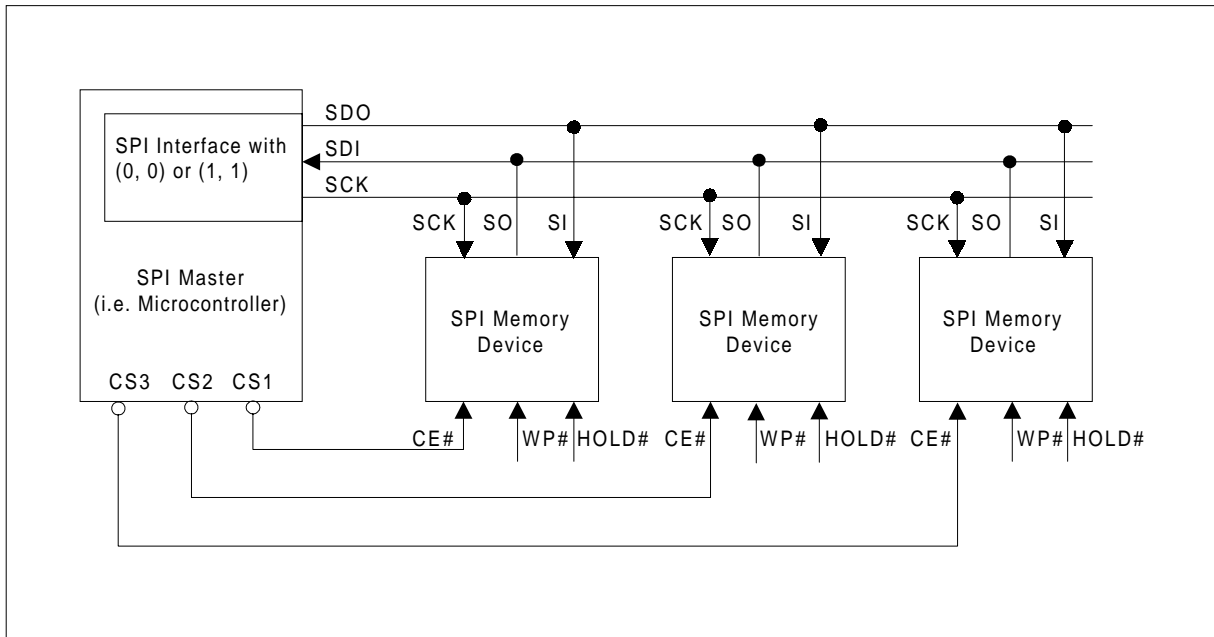
**SPI MODES DESCRIPTION**

Multiple Pm25LV512A/010A/020/040 devices can be serially connected onto the SPI serial bus controlled by a SPI Master i.e. microcontroller as shown in Figure 1. The devices support either of the two SPI modes:

- Mode 0 (0, 0)
- Mode 3 (1, 1)

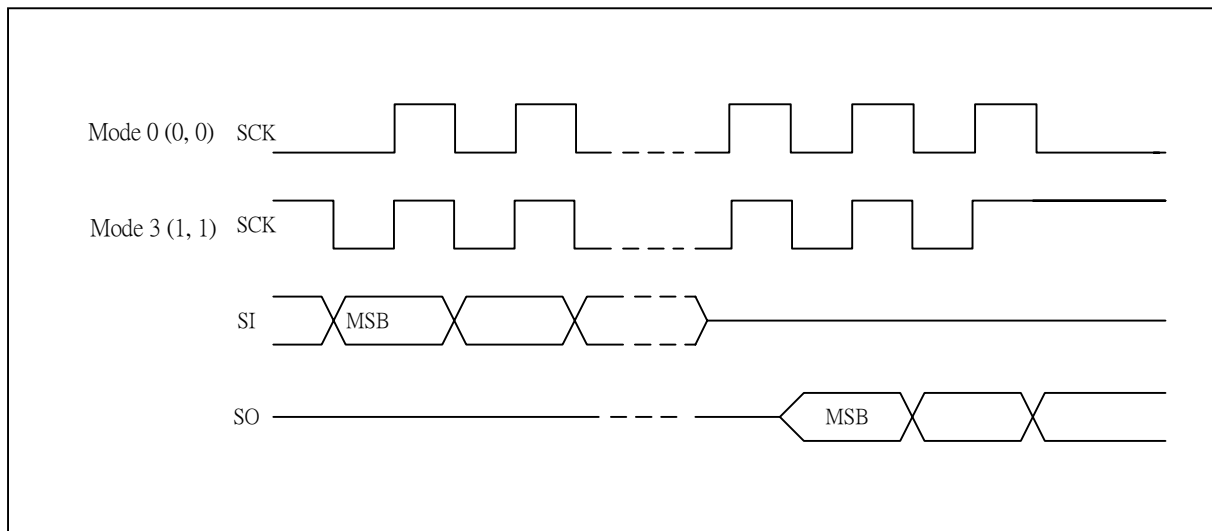
The difference between these two modes is the clock polarity when the SPI master is in Stand-by mode: the serial clock remains at “0” (SCK = 0) for Mode 0 and the clock remains at “1” (SCK = 1) for Mode 1. Please refer to Figure 2. For both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

**Figure 1. Connection Diagram among SPI Master and SPI Slaves (Memory Devices)**



Note: 1. The Write Protect (WP#) and Hold (HOLD#) signals should be driven, High or Low as appropriate.

**Figure 2. SPI Modes Supported**



## REGISTERS

The Pm25LV512A/010A/020/040 are designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of Motorola MC68HCxx series of microcontrollers or all the SPI interface equipped system controllers.

The devices have two superset features can be enabled through the specific software instructions and Configuration Register:

1. Configurable sector size: The memory array of Pm25LV512A/010A are divided into uniform 4 Kbyte sectors or uniform 32 Kbyte blocks (sector group - consists of eight adjacent sectors). The memory array of Pm25LV020/040 are divided into uniform 4 Kbyte sectors or uniform 64 Kbyte blocks (sector group - consists of sixteen adjacent sectors).

2. The Pm25LV010A/020/040 have an option to configure the 4 Kbyte bottom sector (Sector 0) into four 1 Kbyte smaller sectors (Sector 0\_0, Sector 0\_1, Sector 0\_2 and Sector 0\_3). The finer granularity sector size architecture allows user to update data more efficiently. This feature allows user to eliminate the need of additional serial EEPROM.

Refer to Table 1 for Configuration Register and Table 2 for Configuration Register Bit Definition.

**Table 1. Configuration Register Format - Pm25LV010A/020/040**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	SP0_3	SP0_2	SP0_1	SP0_0	SCFG

**Table 2. Configuration Register Bit Definition**

Bit	Name	Definition	Read/Write
Bit 0	SCFG	Sector Configuration: "0" indicates the bottom sector is one 4 Kbyte sector (default) "1" indicates the bottom sector is broken down to four 1 Kbyte sectors This feature can be implemented only when BP0,BP1&BP2 of status register were enabled to "1" which is in protection mode.	R/W
Bit 1	SP0_0	1 Kbyte Sector 0_0 Protection: "0" indicates sector protection is disabled (default) "1" indicates sector protection is enabled	R/W
Bit 2	SP0_1	1 Kbyte Sector 0_1 Protection: "0" indicates sector protection is disabled (default) "1" indicates sector protection is enabled	R/W
Bit 3	SP0_2	1 Kbyte Sector 0_2 Protection: "0" indicates sector protection is disabled (default) "1" indicates sector protection is enabled	R/W
Bit 4	SP0_3	1 Kbyte Sector 0_3 Protection: "0" indicates sector protection is disabled (default) "1" indicates sector protection is enabled	R/W
Bit 5 - 6	RES	Reserved for future (don't care)	N/A
Bit 7	RES	Reserved for future (don't use)	N/A

## **REGISTERS (CONTINUED)**

### **CONFIGURATION REGISTER (Pm25LV010A/020/040)**

The Configuration Register is built by latches need to be set each time after power-up before enabling the 1 Kbyte smaller sector size and 1 Kbyte sector write protection. The Bit 0 - Bit 7 of Configuration Register are set as "0"s after power-up reset. Therefore, the devices will be always set as normal mode - the bottom sector set as 4 Kbyte by default after power-up to maintain the backward-compatibility.

The function of Configuration Register is described as following:

**SCFG bit:** The 1 Kbyte smaller sector mode is enabled by writing "1" to SCFG bit, then Sector 0 is configured as Sector 0\_0, Sector 0\_1, Sector 0\_2 and Sector 0\_3. A Sector Erase (SECTOR\_ER) instruction can be used to erase any one of those four 1 Kbyte sectors. The SCFG bit will be reset "0" state automatically at power on stage. Thus, the 1 Kbyte smaller sector mode is disabled at power on till SCFG bit was set.

The SCFG bit only can be enabled to "1" when BP0, BP1&BP2 of status register were "1" state which in protection mode. On the other word, SCFG bit will be cleared to "0" state when BPx were "0" to disable the protection mode.

**SP0\_x bits:** The write protection to those four 1 Kbyte sectors can be activated by writing "1"s to the SP0\_0, SP0\_1, SP0\_2 and SP0\_3 bits. The 1 Kbyte sector write protection function can only be enabled when the SCFG is also enabled.

The Write Configuration Register (WRCR) instruction can be used to write "0"s or "1"s into Configuration Register. And the Read Configuration Register (RDCR) instruction can be used to read the setting of Configuration Register. Refer to Table 8 for Instruction Set.

### **STATUS REGISTER**

The Status Register contains WIP and WEL status bits to indicate the status of the devices, the Block Protection Bits (BP0, BP1 and BP2 (Pm25LV040 only)) to define the portion of memory blocks to be write protected,

and SRWD control bits to be set for status register write protection. Refer to Table 3 and Table 4 for Status Register Format and Status Register Bit Definition.

The BP0, BP1, BP2, and SRWD are non-volatile memory cells that can be written by Write Status Register (WRSR) instruction. The default value of BP0, BP1, BP2, and SRWD bits were set as "0" at factory. Once those bits are written as "0" or "1", it will not be changed by devices power-up or power-down until next WRSR instruction alters its value. The Status Register can be read by Read Status Register (RDSR) instruction for its value and status. Refer to Table 8 for Instruction Set.

The function of Status Register is described as following:

**WIP bit:** The Write In Progress (WIP) bit can be used to detect the progress or completion of program or erase operation. When WIP bit is "0", the devices are ready for write status register, program or erase operation. When WIP bit is "1", the devices are busy.

**WEL bit:** The Write Enable Latch (WEL) bit indicates the status of internal write enable latch. When WEL bit is "0", the write enable latch is disabled, all write operations include write status register, write configuration register, page program, sector erase, block and chip erase operations are inhibited. When WEL bit is "1", the write enable latch is enabled. Then write operations are allowed. The WEL bit is enabled by Write Enable (WREN) instruction. All write register, program and erase instructions must be preceded by a WREN instruction every time. The WEL bit can be disabled by Write Disable (WRDI) instruction or automatically return to reset state after the completion of a write instruction.

**BP2, BP1, BP0 bits:** The Block Protection (BP2 (Pm25LV040 only), BP1, BP0) bits are used to define the portion of memory area to be protected. Refer to Table 5 and Table 6 Block Write Protection Bits Setting for Pm25LV512A/010A/020 and Pm25LV040. When one of the combination of BP2, BP1 and BP0 bits were set as "1", the relevant memory area is protected. Any program or erase operation to that area will be prohibited. Especially, the Chip Erase (CHIP\_ER) instruction is executed only if all the Block Protection Bits are set as "0"s.

If SCFG bit was enabled to support 1KB x4 sectors on Sector 0, Sector 0's protection status will respect SP0\_x in Configuration Register and ignore BPx bits status whatever protection status.

**REGISTERS (CONTINUED)**

**SRWD bit:** The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to "0", the Status Register is not write protected. When the SRWD is set to "1" and the

WP# is pulled low ( $V_{IL}$ ), the non-volatile bits of Status Register (SRWD, BP2, BP1, BP0) become read-only and the WRSR instruction will be prohibited. If the SRWD is set to "1" but WP# is pulled high ( $V_{IH}$ ), the Status Register is still changeable by WRSR instruction.

**Table 3. Status Register Format**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRWD	0	0	BP2	BP1	BP0	WEL	WIP

**Table 4. Status Register Bit Definition**

Bit	Name	Definition	Read-Write	Non-Volatile bit
Bit 0	WIP	Write In Progress Bit: "0" indicates the device is ready "1" indicates the write cycle is in progress and the device is busy	R	No
Bit 1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W	No
Bit 2	BP0	Block Protection Bit: (See Table 5 and Table 6 for details) "0" indicates the specific blocks are not write protected (default) "1" indicates the specific blocks are write protected	R/W	Yes
Bit 3	BP1			
Bit 4	BP2			
Bits 5 - 6	N/A	Reserved: Always "0"s	N/A	
Bit 7	SRWD	Status Register Write Disable: (See Table 7 for details) "0" indicates the Status Register is not write protected (default) "1" indicates the Status Register is write protected	R/W	Yes

**Table 5. Block Write Protect Bits for Pm25LV512A/010A/020**

Status Register Bits		Protected Memory Area		
BP1	BP0	Pm25LV512A	Pm25LV010A	Pm25LV020
0	0	None	None	None
0	1	None	Upper quarter (Block 3) 018000h - 01FFFFh	Upper quarter (Block 3) 030000h - 03FFFFh
1	0	None	Upper half (Block 2 & 3) 010000h - 01FFFFh	Upper half (Block 2 & 3) 020000h - 03FFFFh
1	1	All Blocks 000000h - 00FFFFh	All Blocks 000000h - 01FFFFh	All Blocks 000000h - 03FFFFh



**REGISTERS (CONTINUED)**
**Table 6. Block Write Protect Bits for Pm25LV040**

Status Register Bits			Protected Memory Area
BP2	BP1	BP0	Pm25LV040
0	0	0	None
0	0	1	Upper eighth (Block 7): 070000h - 07FFFFh
0	1	0	Upper quarter (Block 6 and 7): 060000h - 07FFFFh
0	1	1	Upper half (Block 4 and 7): 040000h - 07FFFFh
1	0	0	All Blocks (Block 0 to 7): 000000h - 03FFFFh
1	0	1	
1	1	0	
1	1	1	

**PROTECTION MODE**

The Pm25LV512A/010A/020/040 have two protection modes: hardware write protection and software write protection to prevent any irrelevant operation under a possible noisy environment and protect the data integrity.

**HARDWARE WRITE PROTECTION**

The devices provide two hardware write protection features:

- When input program instruction, the input clock pulses must be 32 clock pulses for command and address, and a multiple of eight for 1 to 256 of data before execution of programming. Other write instruction must fit in with the number of clock pulse what the instruction requirement before the execution. Any incomplete instruction command sequence will be ignored.
- Write inhibit is 2.1V, all write sequence will be ignored when Vcc drop to 2.1V and lower.
- The devices feature a Write Protection (WP#) pin to provide a hardware write protection method for BP2, BP1, BP0 and SRWD in the Status Register.
  - When the WP# is pulled low ( $V_{IL}$ ), the Status Register is write protected if the SRWD bit is enabled (Refer to Table 7 for Hardware Write Protection on Status Register). Hence part or whole memory area can be write protected depends on the setting of BP2, BP1 and BP0 bits.
  - When the WP# is pulled high ( $V_{IH}$ ), the Status Register is not protected, BP2, BP1, BP0 and SRWD can be changed.

**SOFTWARE WRITE PROTECTION**

The Pm25LV512A/010A/020/040 also provide two software write protection features:

- Before the execution of any program, erase or write status register instruction, the Write Enable Latch (WEL) bit must be enabled by execution of the Write Enable (WREN) instruction. If the WEL bit is not enabled first, the program, erase or write register instruction will be ignored.
- The Block Protection (BP2, BP1, BP0) bits allow part or whole memory area to be write protected.

**Table 7. Hardware Write Protection on Status Register**

SRWD	WP#	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

## DEVICE OPERATION

The Pm25LV512A/010A/020/040 utilize an 8-bit instruction register. Refer to Table 8 Instruction Set for the detail Instructions and Instruction Codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first on Serial Data Input (SI). The input data on SI is latched on the rising edge of Serial Clock (SCK) after the Chip Enable (CE#) is driven low ( $V_{IL}$ ).

Every instruction sequence starts with a one-byte instruction code and might be followed by address bytes, data bytes, or address bytes and data bytes depends on the type of instruction. The CE# must be driven high ( $V_{IH}$ ) after the last bit of the instruction sequence has been shifted in.

**Table 8. Instruction Set**

Instruction Name	Instruction Format	Hex Code	Operation
WREN	0000 0110	06h	Write Enable
WRDI	0000 0100	04h	Write Disable
RDSR	0000 0101	05h	Read Status Register
WRSR	0000 0001	01h	Write Status Register
READ	0000 0011	03h	Read Data Bytes from Memory at Normal Read Mode
FAST_READ	0000 1011	0Bh	Read Data Bytes from Memory at Fast Read Mode
RDID	1010 1011	ABh	Read Manufacturer and Product ID
JEDEC ID READ*1	1001 1111	9Fh	Read Manufacturer and Product ID by JEDEC ID Command
PAGE_PROG	0000 0010	02h	Page Program Data Bytes Into Memory
RDCR	1010 0001	A1h	Read Configuration Register
WRCR	1111 0001	F1h	Write Configuration Register
SECTOR_ER	1101 0111	D7h	Sector Erase
BLOCK_ER	1101 1000	D8h	Block Erase
CHIP_ER	1100 0111	C7h	Chip Erase

Note \*1 : Pm25LV512A do not support JEDEC ID READ instruction.

## HOLD OPERATION

The HOLD# is used in conjunction with the CE# to select the Pm25LV512A/010A/020/040. When the devices are selected and a serial sequence is underway, HOLD# can be used to pause the serial communication

with the master device without resetting the serial sequence. To pause, the HOLD# must be brought low while the SCK signal is low. To resume serial communication, the HOLD# is brought high while the SCK signal is low (SCK may still toggle during HOLD). Inputs to the SI will be ignored while the SO is in the high impedance state.

**DEVICE OPERATION (CONTINUED)**

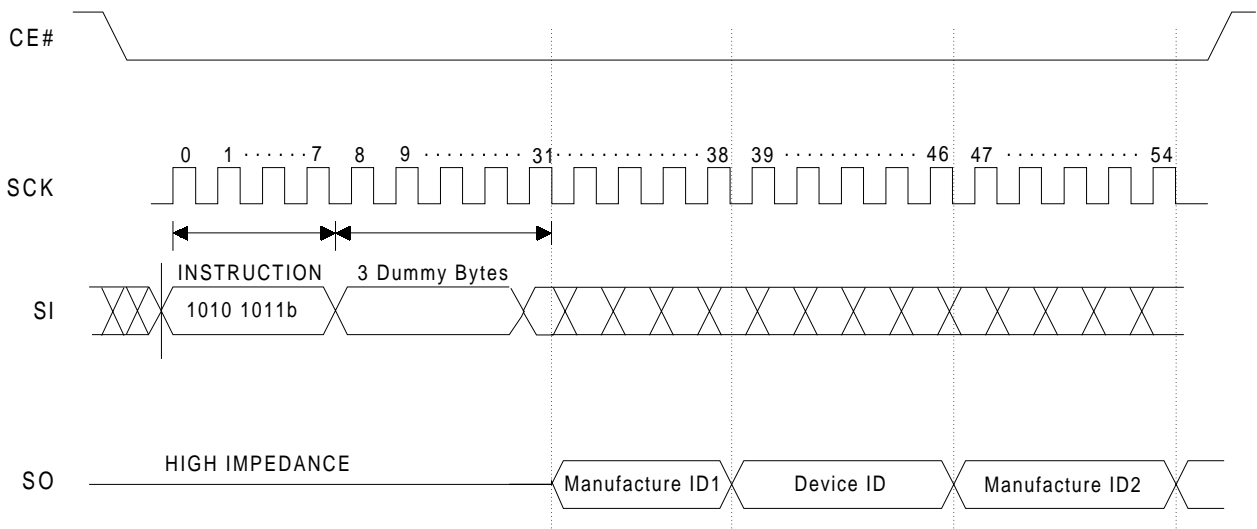
**READ PRODUCT IDENTIFICATION OPERATION**

The Read Product Identification (RDID) instruction allows the user to read the manufacturer and product ID of the devices. Refer to Table 9 Product Identification for pFLASH™ manufacturer ID and device ID. The RDID instruction code is followed by three dummy bytes, each bit being latched-in on SI during the rising edge of SCK. Then the first manufacturer ID (9Dh) is shifted out on SO with the MSB first, followed by the device ID and the second manufacturer ID (7Fh), each bit been shifted out during the falling edge of SCK. If the CE# stays low after the last bit of second manufacturer ID is shifted out, the manufacturer ID and device ID will be looping until the pulled high of CE# signal.

**Table 9. Product Identification**

Product Identification		Data
Manufacturer ID	First Byte	9Dh
	Second Byte	7Fh
Device ID:		
Pm25LV512A		7Bh
Pm25LV010A		7Ch
Pm25LV020		7Dh
Pm25LV040		7Eh

**Figure 3. Read Product Identification Sequence**



**DEVICE OPERATION (CONTINUED)**

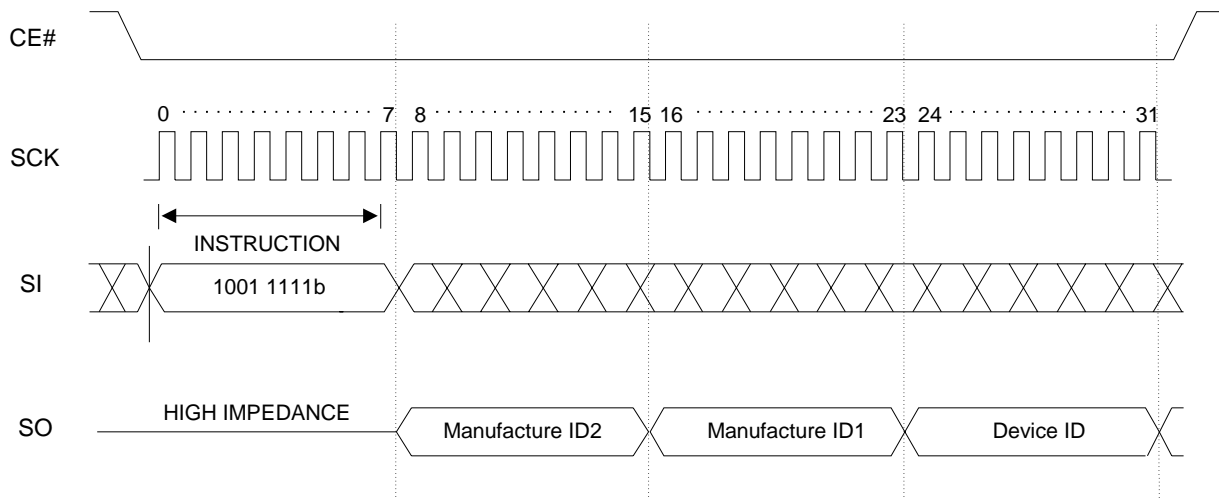
**READ PRODUCT IDENTIFICATION BY JEDEC ID COMMAND**

The JEDEC ID READ instruction allows the user to read the manufacturer and product ID of the devices. Refer to Table 9 Product Identification for pFLASH™ manufacturer ID and device ID. The second manufacturer ID (7Fh) is shifted out on SO with the MSB first after JEDEC ID READ command input, followed by the first manufacturer ID (9Dh) and the device ID, each bit been shifted out during the falling edge of SCK.

If the CE# stays low after the last bit of device ID is shifted out, the manufacturer ID and device ID will be looping until the pulled high of CE# signal.

Pm25LV512A do not support this JEDEC ID READ instruction.

**Figure 4. Read Product Identification by JEDEC ID READ Sequence**



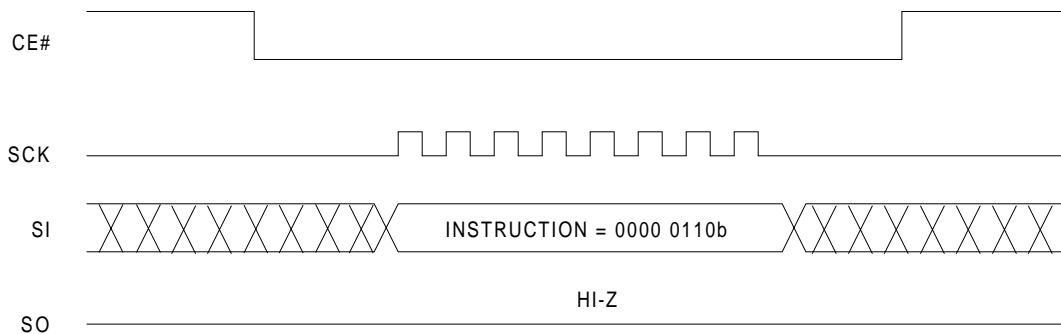
**DEVICE OPERATION (CONTINUED)**

**WRITE ENABLE OPERATION**

The Write Enable (WREN) instruction is used to set the Write Enable Latch (WEL) bit. The WEL bit of the Pm25LV512A/010A/020/040 are set as write disable state after power-up. The WEL bit must be write enabled before any write operation includes sector, block and

chip erase, page program, write status register, and write configuration register operations. The WEL bit will be reset back to write disable state automatically after the completion of a write operation. The WREN instruction is required before any above instruction is executed.

**Figure 5. Write Enable Sequence**

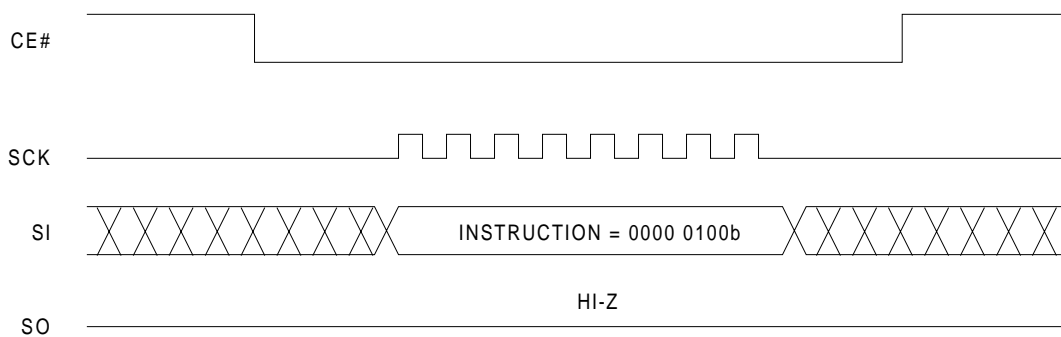


**WRITE DISABLE OPERATION**

To protect the device against inadvertent writes, the Write Disable (WRDI) instruction resets the WEL bit and disables all write instructions. The WRDI instruction is not

required after the execution of a write instruction. The WEL will be automatically reset.

**Figure 6. Write Disable Sequence**



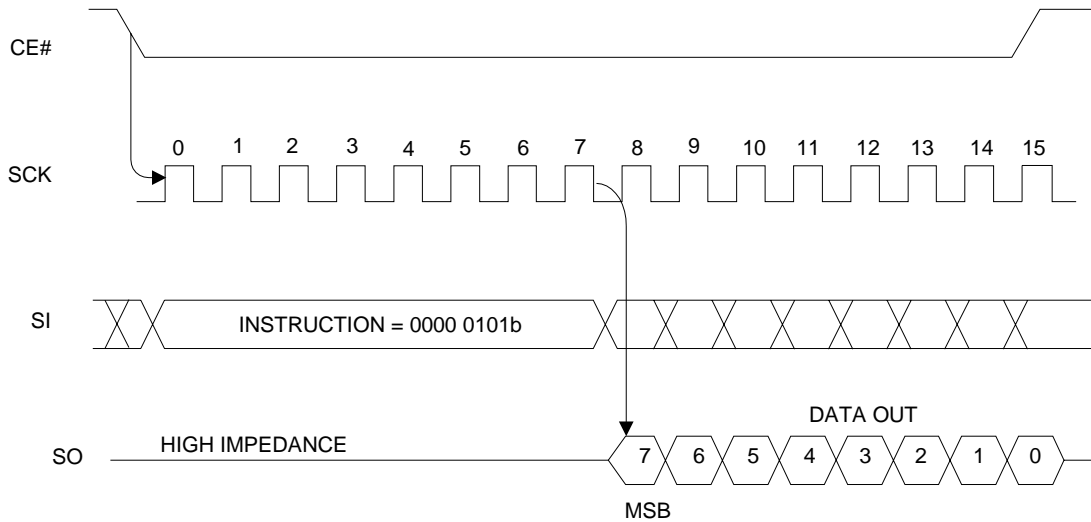
**DEVICE OPERATION (CONTINUED)**

**READ STATUS REGISTER OPERATION**

The Read Status Register (RDSR) instruction provides access to the status register. During the execution of a program, erase or write status register operation, all other

instructions will be ignored except the RDSR instruction can be used for detecting the progress or completion of the operations by reading the WIP bit of status register.

**Figure 7. Read Status Register Sequence**

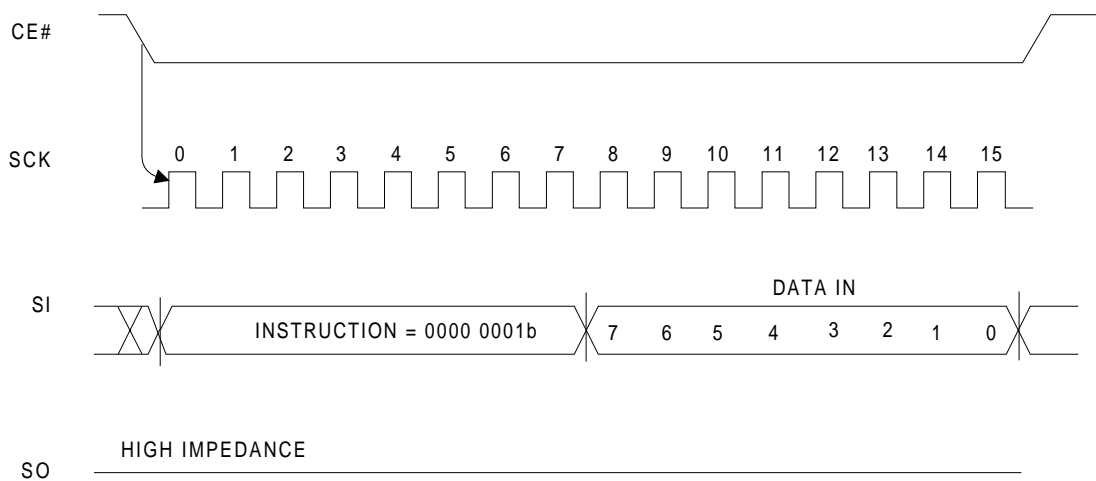


**WRITE STATUS REGISTER OPERATION**

The Write Status Register (WRSR) instruction allows the user to enable or disable the block protection and status register write protection features by writing "0"s

or "1"s into those non-volatile BP2, BP1, BP0 and SRWD bits. The erase operation for those non-volatile bits are not required.

**Figure 8. Write Status Register Sequence**



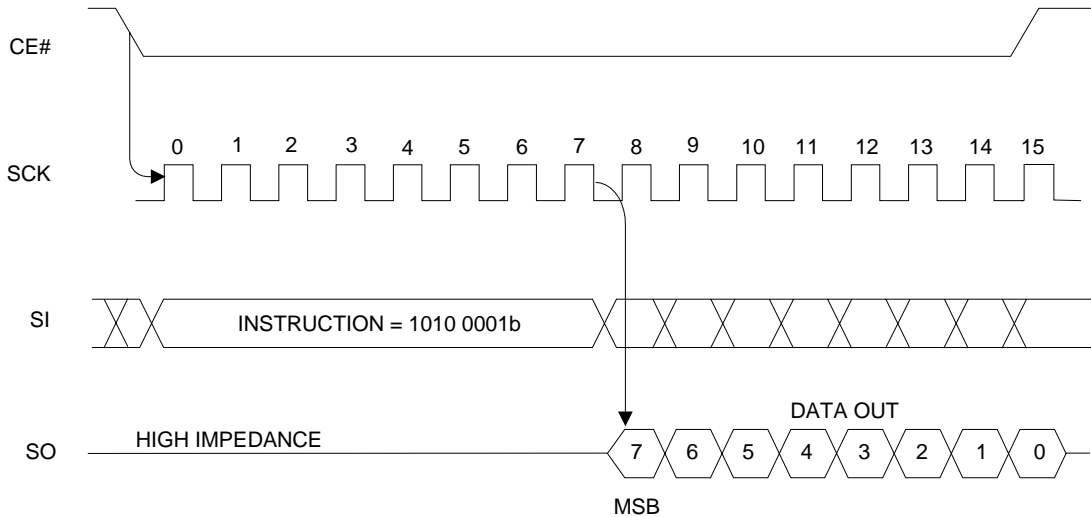
**DEVICE OPERATION (CONTINUED)**

**READ CONFIGURATION REGISTER OPERATION**

The Read Configuration Register (RDCR) instruction provides access to the Configuration Register. This instruction can be used to verify the configuration setting of

bottom Sector 0 and the write protection setting for each individual 1 Kbyte sector (Sector 0\_0 ~ Sector 0\_3) within the Sector 0.

**Figure 9. Read Configuration Register Sequence**

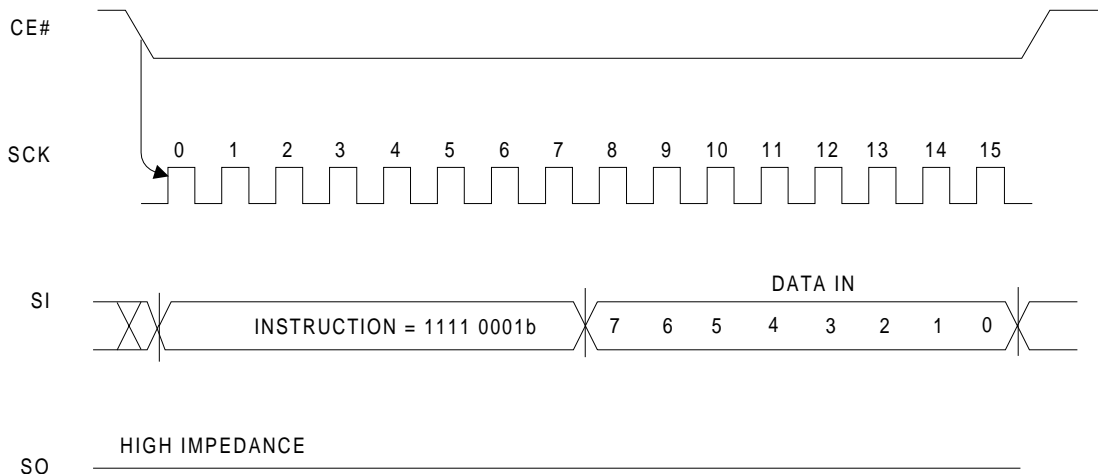


**WRITE CONFIGURATION REGISTER OPERATION**

The Write Configuration Register (WRCR) instruction allows user to enable or disable four smaller 1K byte sectors and protection for each 1K byte sector by writing "0"s or "1"s into SCFG and SP0\_3 ~SP0\_1 in the configuration register. please refer table 2 for details.

Do not require WREN command before this WRCR operation. Because Configuration Register is a data latch architecture.

**Figure 10. Write Configuration Register Sequence**



**DEVICE OPERATION (CONTINUED)**

**READ DATA OPERATION**

The Read Data (READ) instruction is used to read memory data of Pm25LV512A/010A/020/040 under normal mode running up to 33 MHz.

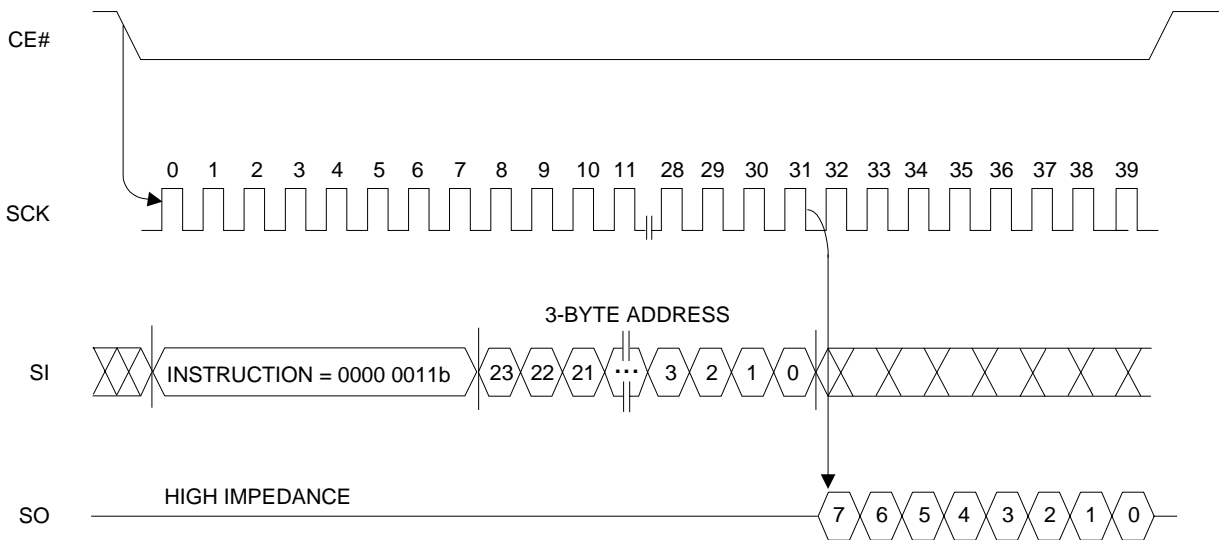
The READ instruction is activated by pulling the CE# line of the selected device to low ( $V_{IL}$ ), and the READ instruction code is transmitted via the SI line followed by three bytes address (A23 - A0) to be read. There are total 24 address bits will be shifted in, only the  $A_{MS}$  (most-significant address) - A0 will be decoded and the rest of A23 -  $A_{MS}$  can be don't cared. Refer to Table 10 for the related Address Key. Upon completion, any data on the SI will be ignored.

The first byte data D7 - D0 addressed (can be at any location) is then shifted out onto the SO line. A single byte data or up to whole memory array can be read out in one READ instruction. The address is automatically incremented to the next higher address after each byte of data is shifted out. The read operation can be terminated any time by driving the CE# high ( $V_{IH}$ ) after the data comes out. When the highest address of the devices is reached, the address counter will roll over to the 000000h address allowing the entire memory to be read in one continuous READ instruction.

**Table 10. Address Key**

Address	Pm25LV512A	Pm25LV010A	Pm25LV020	Pm25LV040
$A_N$	A15 - A0	A16 - A0	A17 - A0	A18 - A0
Don't Care Bits	A23 - A16	A23 - A17	A23 - A18	A23 - A19

**Figure 11. Read Data Sequence**





**DEVICE OPERATION (CONTINUED)**

**FAST READ DATA OPERATION**

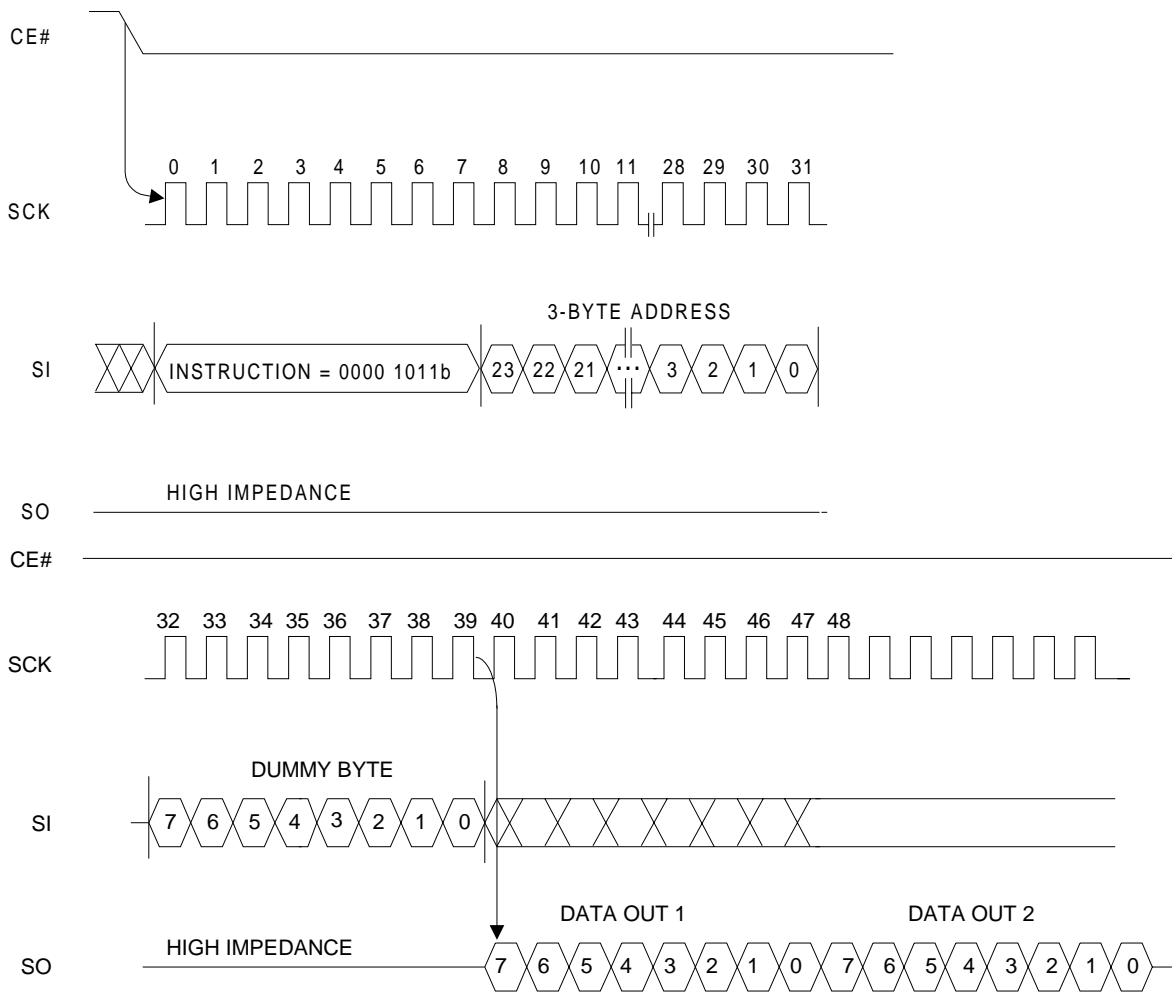
The Pm25LV512A/010A/020/040 also feature a Fast Read (FAST\_READ) instruction. This FAST\_READ instruction is used to read memory data in 100 MHz clock rate where the FAST\_READ instruction proceeding.

The devices are first selected by driving CE# low ( $V_{IL}$ ). The FAST\_READ instruction code followed by three bytes address (A23 - A0) and a dummy byte (8 clocks) is transmitted via the SI line, each bit being latched-in during the rising edge of SCK. Then the first data byte

addressed is shifted out on SO line, each bit being shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address allowing the entire memory to be read with a single FAST\_READ instruction. The FAST\_READ instruction is terminated by driving CE# high ( $V_{IH}$ ).

**Figure 12. Fast Read Data Sequence**



**DEVICE OPERATION (CONTINUED)**

**PAGE PROGRAM OPERATION**

The Page Program (PAGE\_PROG) instruction allow up to 256 bytes data to be programmed into memory in one program operation page by page. The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP2, BP1, BP0) bits. A PAGE\_PROG instruction attempts to program into a page which is write protected will be ignored. Before the execution of PAGE\_PROG instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The PAGE\_PROG instruction is activated, after the CE# is pulled low to select the device and staying low during the entire instruction sequence, by shifting in the PAGE\_PROG instruction code, three address bytes and program data (1 to 256 bytes) to be programmed via the SI line. Program operation will start immediately after the CE# is driven high. Chip Select (CE#) must be driven high after the eighth bit of last data byte has been latch in, otherwise the PAGE\_PROG instruction will not be executed.

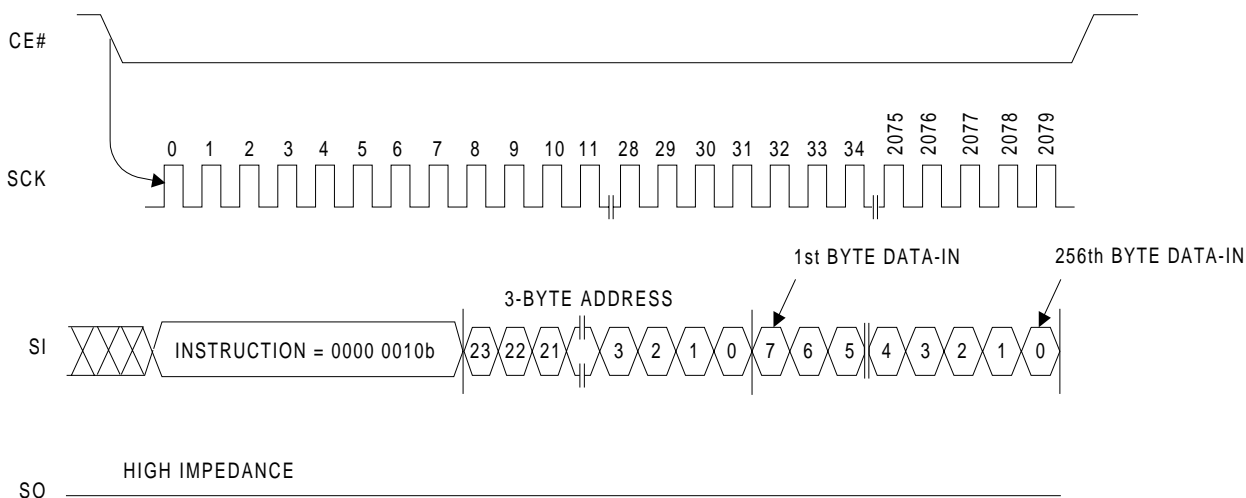
The internal control logic automatically handles the programming voltages and timing. During a program

operation, all instructions will be ignored except the RDSR instruction. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register through a RDSR instruction. If WIP bit = "1", the program operation is still in progress. If WIP bit = "0", the program operation has completed.

A single PAGE\_PROG instruction programs 1 to 256 consecutive bytes within a page if it is not write protected. If more than 256 bytes data are sent to the devices, the address counter will roll over on the same page and the previously latched data are discarded and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the same page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

A program operation can alter "1"s into "0"s, but an erase operation is required to change "0"s back to "1"s. The same byte cannot be reprogrammed without erasing the whole sector or block first.

**Figure 13. Page Program Sequence**



## **DEVICE OPERATION (CONTINUED)**

### **ERASE OPERATION**

The memory array of Pm25LV512A/010A is organized into uniform 4 Kbyte sectors or 32 Kbyte uniform blocks (sector group - consists of eight adjacent sectors). The memory array of Pm25LV020/040 are organized into uniform 4 Kbyte sectors or 64 Kbyte uniform blocks (sector group - consists of sixteen adjacent sectors). The Pm25LV010A/020/040 of bottom sector (Sector 0) of the devices can be configured into four 1 Kbyte smaller sectors.

Before a byte can be reprogrammed, the sector or block which contains this byte must be erased first. In order to erase the devices, there are three erase instructions include Sector Erase (SECTOR\_ER), Block Erase (BLOCK\_ER) and Chip Erase (CHIP\_ER) instructions can be used. A sector erase operation allows to erase any individual sector without affecting the data in others. A block erase operation allows to erase any individual block. And a chip erase operation allows to erase the whole memory array of the devices. Pre-programs the devices are not required prior to a sector erase, block erase or chip erase operation.

### **SECTOR ERASE OPERATION**

A SECTOR\_ER instruction erases a 4 Kbyte sector or a 1 Kbyte smaller sector (Sector 0\_3, Sector 0\_2, Sector 0\_1, Sector 0\_0) if the bottom Sector 0 has been configured as four smaller sectors. Before the execution of SECTOR\_ER instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction. The WEL will be reset automatically after the completion of sector erase operation.

The SECTOR\_ER instruction is entered, after the CE# is pulled low to select the device and staying low during the entire instruction sequence, by shifting in the SECTOR\_ER instruction code and three address bytes via the SI. Erase operation will start immediately after the CE# is pulled high, otherwise the SECTOR\_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 13 for Sector Erase Sequence.

During a erase operation, all instruction will be ignored except the Read Status Register (RDSR) instruction. The progress or completion of the erase operation can be determined by reading the WIP bit in Status Register through a RDSR instruction. If WIP bit = "1", the erase operation is still in progress. If WIP bit = "0", the erase operation has been completed.

### **BLOCK ERASE OPERATION**

A Block Erase (BLOCK\_ER) instruction erases a 32 Kbyte block for the Pm25LV512A/010A or a 64 Kbyte block for the Pm25LV020/040. Before the execution of BLOCK\_ER instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction. The WEL will be reset automatically after the completion of block erase operation.

The BLOCK\_ER instruction is entered, after the CE# is pulled low to select the device and staying low during the entire instruction sequence, by shifting in the BLOCK\_ER instruction code and three address bytes via the SI. Erase operation will start immediately after the CE# is pulled high, otherwise the BLOCK\_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 14 for Block Erase Sequence.

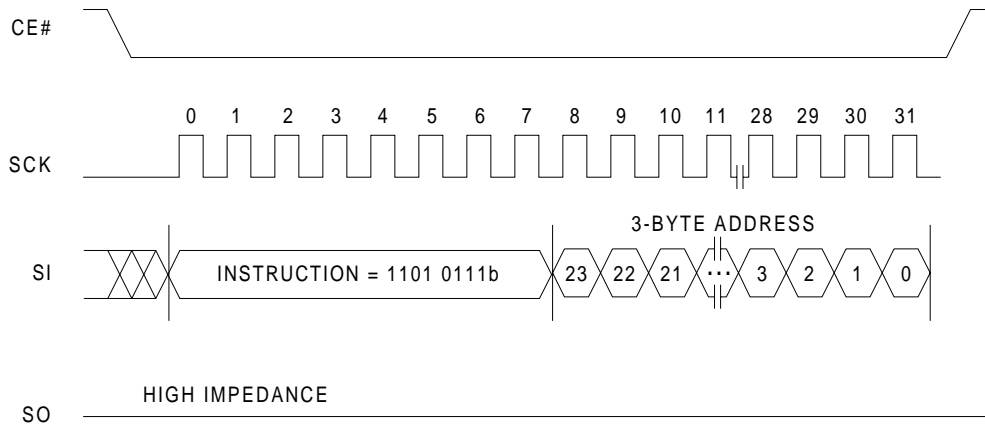
### **CHIP ERASE OPERATION**

A Chip Erase (CHIP\_ER) instruction erases the whole memory array of Pm25LV512A/010A/020/040. Before the execution of CHIP\_ER instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction. The WEL will be reset automatically after the completion of chip erase operation.

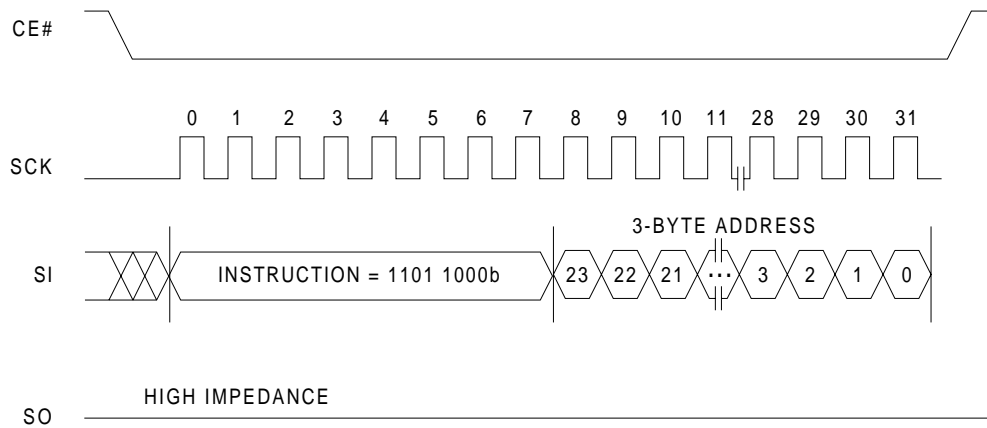
The CHIP\_ER instruction is entered, after the CE# is pulled low to select the device and staying low during the entire instruction sequence, by shifting in the CHIP\_ER instruction code via the SI. Erase operation will start immediately after the CE# is pulled high, otherwise the CHIP\_ER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing. Refer to Figure 15 for Chip Erase Sequence.

**DEVICE OPERATION (CONTINUED)**

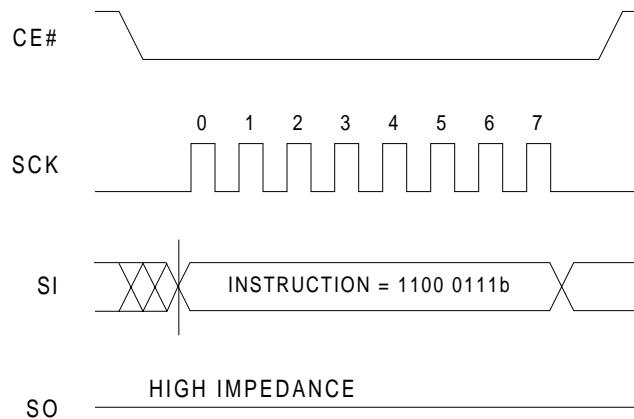
**Figure 14. Sector Erase Sequence**



**Figure 15. Block Erase Sequence**



**Figure 16. Chip Erase Sequence**



**BLOCK/SECTOR ADDRESS**
**Table 11. Block/Sector Addresses of Pm25LV512A/010A**

Memory Density		Block No.	Block Size (Kbytes)	Sector No.	Sector Size (Kbytes)	Address Range
512 Kbit	1 Mbit	Block 0	32	Sector 0 <sup>(1)</sup>	4	000000h - 000FFFh
				Sector 1	4	001000h - 001FFFh
				:	:	:
				Sector 7	4	007000h - 007FFFh
		Block 1	32	Sector 8	4	008000h - 008FFFh
				Sector 9	4	009000h - 009FFFh
				:	:	000000h - 006FFFh
				Sector 15	4	00F000h - 00FFFFh
		Block 2	32	"	"	010000h - 017FFFh
		Block 3	32	"	"	018000h - 01FFFFh

Note: 1. Pm25LV010A support 1KByte small sector - Sector 0 can be configured into four smaller 1 Kbyte sectors (Sector 0\_0: 000000h - 0003FFh, Sector 0\_1: 000400h - 0007FFh, Sector 0\_2: 000800h - 000BFFh, and Sector 0\_3: 000C00h - 000FFFh).

**BLOCK/SECTOR ADDRESS (CONTINUED)**
**Table 12. Block/Sector Addresses of Pm25LV020/040**

Memory Density		Block No.	Block Size (Kbytes)	Sector No.	Sector Size (Kbytes)	Address Range
2 Mbit	4 Mbit	Block 0	64	Sector 0 <sup>(1)</sup>	4	000000h - 000FFFh
				Sector 1	4	001000h - 001FFFh
				:	:	:
				Sector 15	4	00F000h - 00FFFFh
		Block 1	64	Sector 16	4	010000h - 010FFFh
				Sector 17	4	011000h - 011FFFh
				:	:	:
				Sector 31	4	01F000h - 01FFFFh
		Block 2	64	"	"	020000h - 02FFFFh
		Block 3	64	"	"	030000h - 03FFFFh
		Block 4	64	"	"	040000h - 04FFFFh
		Block 5	64	"	"	050000h - 05FFFFh
		Block 6	64	"	"	060000h - 06FFFFh
		Block 7	64	"	"	070000h - 07FFFFh

Note: 1. Sector 0 can be configured into four smaller 1 Kbyte sectors (Sector 0\_0: 000000h - 0003FFh, Sector 0\_1: 000400h - 0007FFh, Sector 0\_2: 000800h - 000BFFh, and Sector 0\_3: 000C00h - 000FFFh).

**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

Temperature Under Bias		-65°C to +125°C
Storage Temperature		-65°C to +125°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins <sup>(2)</sup>		-0.5 V to $V_{CC} + 0.5 V$
All Output Voltage with Respect to Ground		-0.5 V to $V_{CC} + 0.5 V$
$V_{CC}$ <sup>(2)</sup>		-0.5 V to +6.0 V

**Notes:**

- Stresses under those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device or any other conditions under those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affected device reliability.
- Maximum DC voltage on input or I/O pins are  $V_{CC} + 0.5 V$ . During voltage transitioning period, input or I/O pins may overshoot to  $V_{CC} + 2.0 V$  for a period of time up to 20 ns. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitioning period, input or I/O pins may undershoot GND to -2.0 V for a period of time up to 20 ns.

**DC AND AC OPERATING RANGE**

<b>Part Number</b>	<b>Pm25LV512A/010A/020/040</b>
Operating Temperature	-40°C to +105°C
Vcc Power Supply	2.7 V - 3.6 V

## DC CHARACTERISTICS

Applicable over recommended operating range from:

$T_{AC} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$  (unless otherwise noted).

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{CC1}$	Vcc Active Read Current	$V_{CC} = 3.6\text{V}$ at 33 MHz, SO = Open		10	15	mA
$I_{CC2}$	Vcc Program/Erase Current	$V_{CC} = 3.6\text{V}$ at 33 MHz, SO = Open		15	30	mA
$I_{SB1}$	Vcc Standby Current CMOS	$V_{CC} = 3.6\text{V}$ , CE# = $V_{CC}$			50	$\mu\text{A}$
$I_{SB2}$	Vcc Standby Current TTL	$V_{CC} = 3.6\text{V}$ , CE# = $V_{IH}$ to $V_{CC}$			3	mA
$I_{LI}$	Input Leakage Current	$V_{IN} = 0\text{V}$ to $V_{CC}$			1	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$V_{IN} = 0\text{V}$ to $V_{CC}$ , $T_{AC} = 0^{\circ}\text{C}$ to $105^{\circ}\text{C}$			1	$\mu\text{A}$
$V_{IL}$	Input Low Voltage		-0.5		0.8	V
$V_{IH}$	Input High Voltage		$0.7V_{CC}$		$V_{CC} + 0.3$	V
$V_{OL}$	Output Low Voltage	$2.7\text{V} < V_{CC} < 3.6\text{V}$			0.45	V
$V_{OH}$	Output High Voltage		$I_{OL} = 2.1\text{ mA}$			V
			$I_{OH} = -100\ \mu\text{A}$	$V_{CC} - 0.2$		V



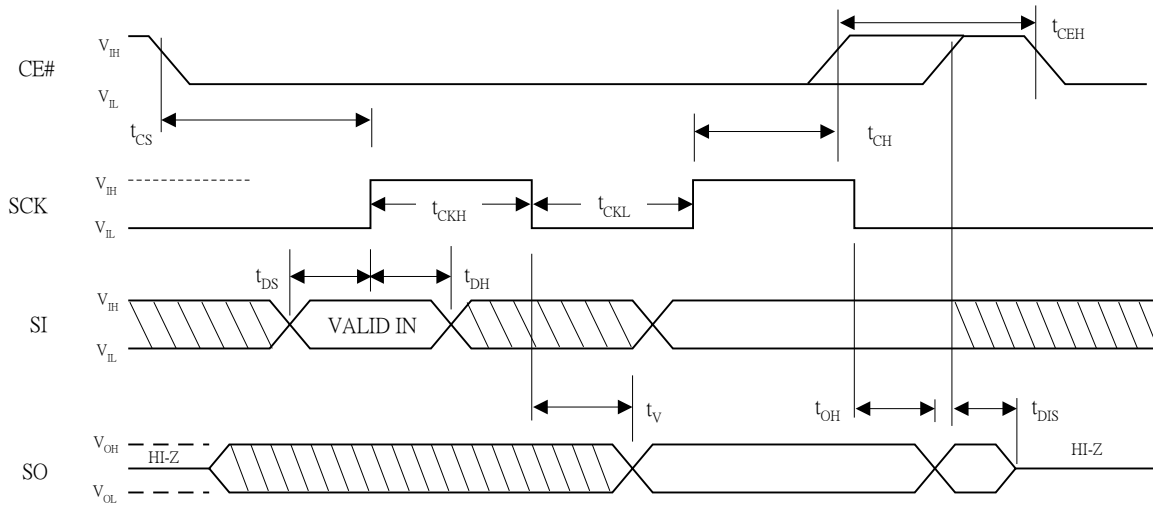
## AC CHARACTERISTICS

Applicable over recommended operating range from  $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$   
 $C_L = 1\text{ TTL Gate}$  and  $10\text{ pF}$  (unless otherwise noted).

Symbol	Parameter	Min	Typ	Max	Units
$f_{CT}$	Clock Frequency for fast read mode	0		100	MHz
$f_C$	Clock Frequency for read mode	0		33	MHz
$t_{RI}$	Input Rise Time			8	ns
$t_{FI}$	Input Fall Time			8	ns
$t_{CKH}$	SCK High Time	4			ns
$t_{CKL}$	SCK Low Time	4			ns
$t_{CEH}$	CE# High Time	25			ns
$t_{CS}$	CE# Setup Time	10			ns
$t_{CH}$	CE# Hold Time	5			ns
$t_{DS}$	Data In Setup Time	2			ns
$t_{DH}$	Data in Hold Time	2			ns
$t_{HS}$	Hold Setup Time	15			ns
$t_{HD}$	Hold Time	15			ns
$t_V$	Output Valid			8	ns
$t_{OH}$	Output Hold Time Normal Mode	0			ns
$t_{LZ}$	Hold to Output Low Z			200	ns
$t_{HZ}$	Hold to Output High Z			200	ns
$t_{DIS}$	Output Disable Time			100	ns
$t_{EC}$	Sector/Block/Chip Erase Time		40	100	ms
$t_{PP}$	Page Program Time		2	5	ms
$t_W$	Write Status Register Time		40	100	ms
$t_{VCS}$	$V_{CC}$ Set-up Time	50			$\mu\text{s}$

**AC CHARACTERISTICS (CONTINUED)**

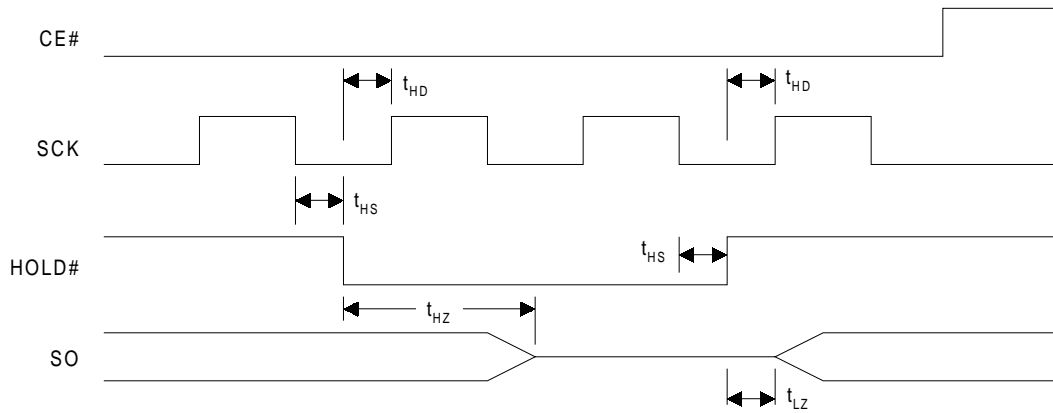
**SERIAL INPUT/OUTPUT TIMING<sup>(1)</sup>**



Note: 1. For SPI Mode 0 (0,0)

**AC CHARACTERISTICS (CONTINUED)**

**HOLD TIMING**

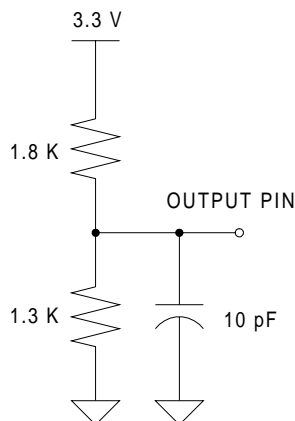


**PIN CAPACITANCE ( f = 1 MHz, T = 25°C )**

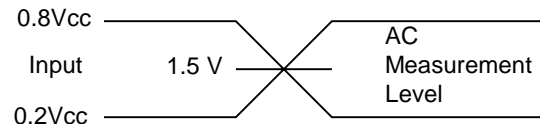
	Typ	Max	Units	Conditions
$C_{IN}$	4	6	pF	$V_{IN} = 0 V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0 V$

Note: These parameters are characterized but not 100% tested.

**OUTPUT TEST LOAD**



**INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL**



- Note: 1. Input Pulse Voltage :  $0.2V_{CC}$  to  $0.8V_{CC}$ .
- 2. Input Timing Reference Voltages :  $0.3V_{CC}$  to  $0.7V_{CC}$ .
- 3. Output Timing Reference Voltage :  $V_{CC}/2$ .

## POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must not be selected (CE# must follow the voltage applied on Vcc) until Vcc reaches the correct value:

- Vcc(min) at Power-up, and then for a further delay of tVCE
- Vss at Power-down

Usually a simple pull-up resistor on CE# can be used to insure safe and proper Power-up and Power-down.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while Vcc is less than the POR threshold value (Vwi) during power up, the device does not respond to any instruction until a time delay of tPUW has elapsed after the moment that Vcc rised above the VWI threshold. However, the correct operation of the device is not guaranteed if, by this time, Vcc is still below Vcc(min). No Write Status

Register, Program or Erase instructions should be sent until the later of:

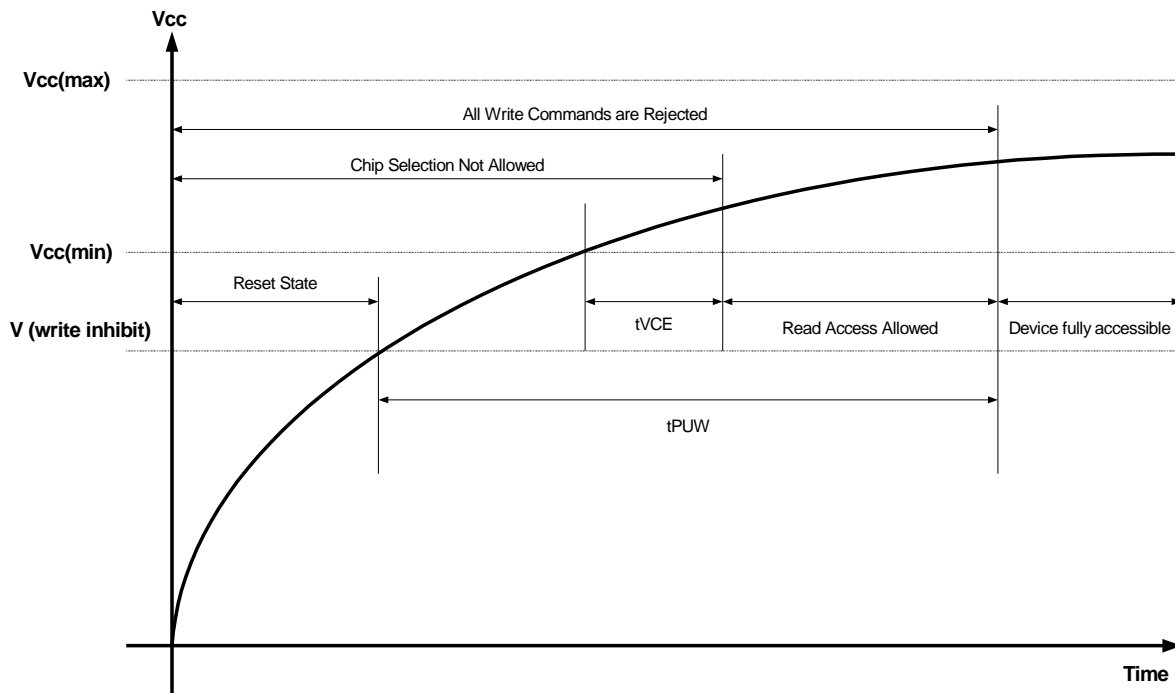
- tPUW after Vcc passed the VWI threshold
- tVCE after Vcc passed the Vcc(min) level

At Power-up, the device is in the following state:

- The device is in the Standby mode
- The Write Enable Latch (WEL) bit is reset

At Power-down, when Vcc drops from the operating voltage, to below the Vwi, all write operations are disabled and the device does not respond to any write instruction.

### Power-up Timing



Symbol	Parameter	Min.	Max.	Unit
t <sub>VCE</sub> <sup>*1</sup>	Vcc(min) to CE# Low	10		us
t <sub>PUW</sub> <sup>*1</sup>	Power-Up time delay to Write instruction	1	10	ms
V <sub>WI</sub> <sup>*1</sup>	Write Inhibit Voltage	2.1	2.3	V

Note : \*1. These parameters are characterized only.

**PROGRAM/ERASE PERFORMANCE**

Parameter	Unit	Typ	Max	Remarks
Sector Erase Time	ms	40	100	From writing erase command to erase completion
Block Erase Time	ms	40	100	From writing erase command to erase completion
Chip Erase Time	ms	40	100	From writing erase command to erase completion
Page Programming Time	ms	2	5	From writing program command to program completion

Note: These parameters are characterized and are not 100% tested.

**RELIABILITY CHARACTERISTICS**

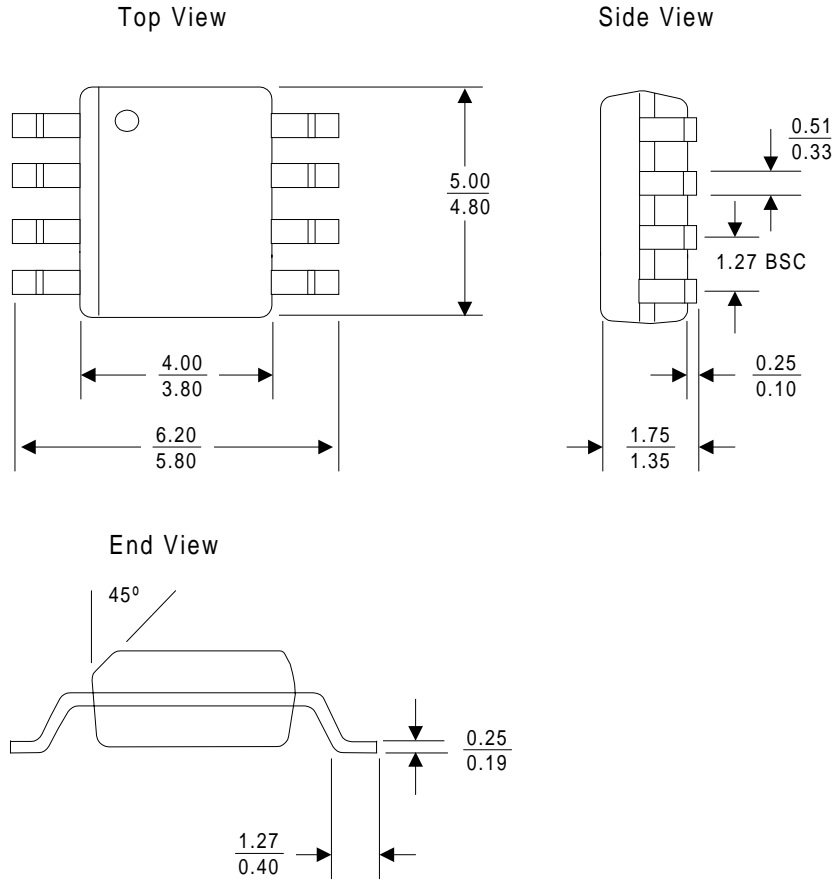
Parameter	Min	Typ	Unit	Test Method
Endurance	200,000		Cycles	JEDEC Standard A117
Data Retention	20		Years	JEDEC Standard A103
ESD - Human Body Model	2,000		Volts	JEDEC Standard A114
ESD - Machine Model	200		Volts	JEDEC Standard A115
ESD - Charged Device Model	1,000		Volts	JEDEC Standard C101-A
Latch-Up	100 + I <sub>CC1</sub>		mA	JEDEC Standard 78

Note: These parameters are characterized and are not 100% tested.

**PACKAGE TYPE INFORMATION**

**8S**

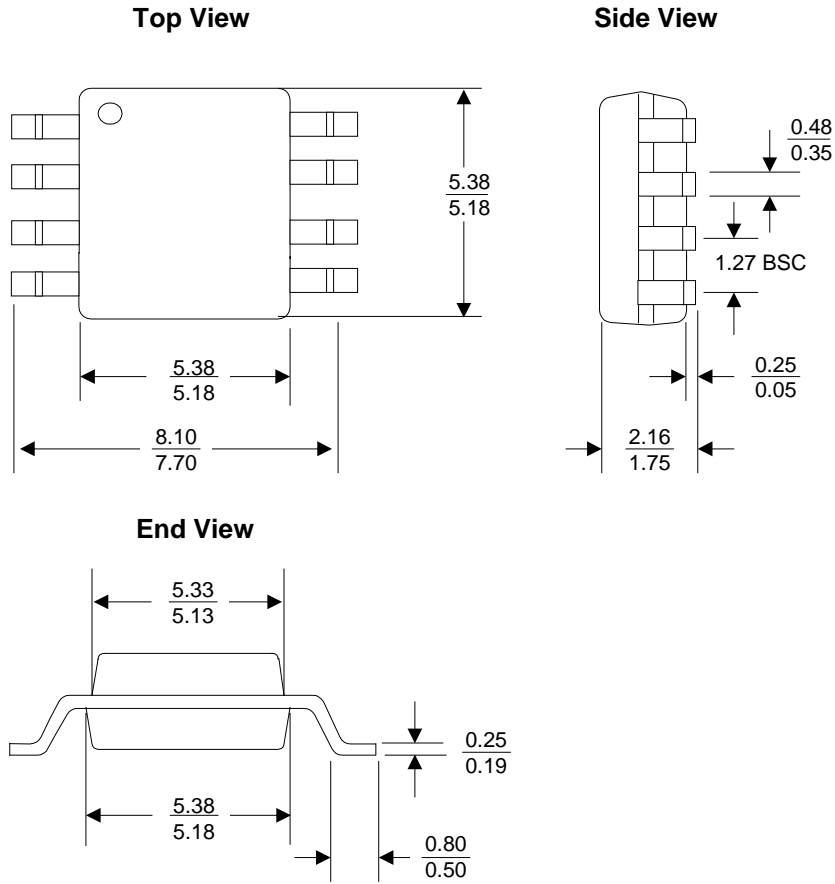
**8-Pin JEDEC 150mil Small Outline Integrated Circuit (SOIC) Package  
(measure in millimeters)**



**PACKAGE TYPE INFORMATION**

**8B**

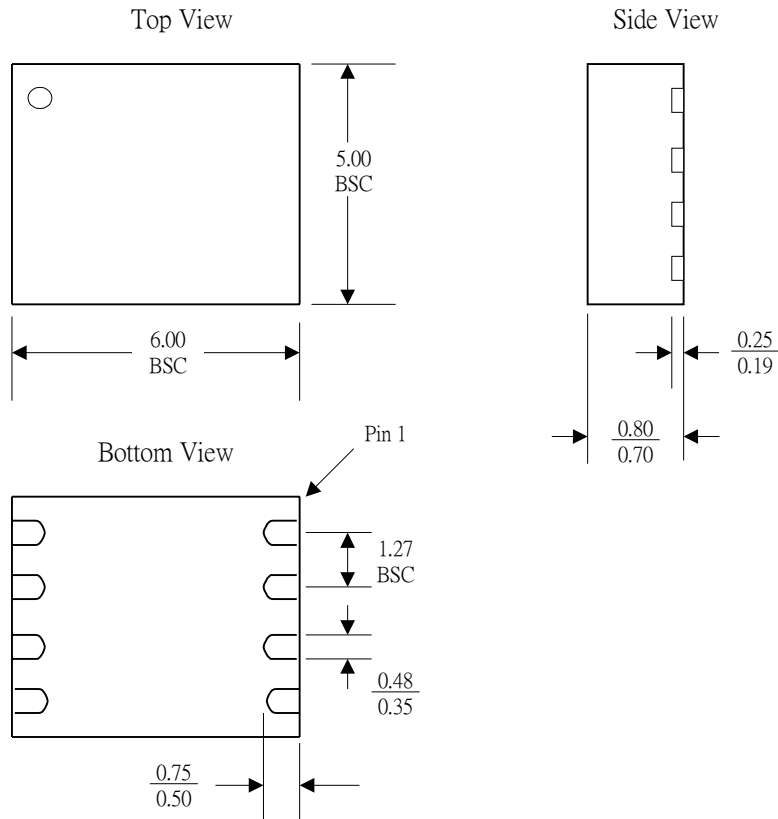
**8-Pin JEDEC 208mil Broad Small Outline Integrated Circuit (SOIC) Package  
(measure in millimeters)**



**PACKAGE TYPE INFORMATION (CONTINUED)**

**8Q**

**8-Contact Ultra-Thin Small Outline No-Lead (WSON) Package (measure in millimeters)**





**REVISION HISTORY**

Date	Revision No.	Description of Changes	Page No.
January, 2004	0.3	Advanced Product Specification	All
March, 2004	0.4	Extend The Range of Operation Temperature	All
August, 2004	0.5	Correct part no for WSON package Register status setting	3 6,7,8
October, 2004	0.6	Correct part no Register setting for small sector feathure	All page 7
January, 2005	0.7	Preliminary version release	
January, 2005	0.8	1. Support 208mil SOIC package 2. Correct read timing for D0 latch by HOST 3. Remove Turbo mode	All
February, 2005	0.9	Support 33MHz Removed bask side metal of WSON Standby current	1,3,15,23,24, 30
May, 2005	1.0	JEDEC ID READ instruction Correct the smaller sector (1KB) feature	6,7,10,12
June, 2005	1.1	Description update for the operation of Configuration Register	8,9,15,16
July, 2005	2.0	Support 75MHz for Fast Read Mode	All
July, 2005	2.1	1. Update fast read speed to 100MHz. 2. Sectore/Block archeticture description. 3. Ordering information - remove non-pbfree parts. 4. Highligh no require WREN before WRCR command. 5. AC measurement conditions.	1,3,16,28
November, 2005	2.3	1. Change AC paramaters for 100MHz spec. Tv 8ns with 10pF Loading, Data In Hold/Setup tiime 2ns(min), Clock high/low time 4ns(min) TRI, TFI, 8ns(max), TDIS 10ns(max) 2. Support Commercial Grade to -40~+85degreeC 3. Partno chage for Pm25LV010 to Pm25LV010A.	3, 24,25
February, 2006	2.4	1. Update endurance to 200K cycle. 2. Update write inhibit spec. to 2.1V . 3. Update ESD CDM spec 1000V.	1,9,28
March, 2006	2.5	1.Change Logo and company name 2.Modified test condition for DC	All 24
March, 2006	2.6	Extend the operated temperature to +105degreeC	3,23,24,25
April, 2006	2.7	1. Update Pm25LV512A in the datasheet 2. Correct tCH definition 3. Power-up timing difinition	All 25,26 28
May, 2006	2.8	Correct the statement of hardware write protection	9
June, 2006	2.9	To declare 'E' pacakge for RoHS compliance	3